Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1287	((703/13) or (703/14) or (703/16) or (703/4)).CCLS.	USPAT	OR	OFF	2005/04/16 18:09
L2	0	1 and (non adj order)	USPAT	OR	ON	2005/04/16 18:09
L3	163	1 and (non same order)	USPAT	OR	ON	2005/04/16 18:09
L4	626931	"4" and event$5	USPAT	OR	ON	2005/04/16 18:09
L5	79	3 and event$5	USPAT	OR	ON	2005/04/16 18:09
L6	8	5 and (real adj number$5)	USPAT	OR	ON	2005/04/16 18:10

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	36	(non-order or (non adj sequencial))	USPAT	OR	ON	2005/04/16 17:41
L2	68	(non-order or (non adj sequencial))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/16 17:41
L3	0	2 and (event same management)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/16 17:42
L4	28	2 and event$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/16 17:46
L5	10	(schedule adj time) and (real adj number)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/16 17:49
L6	155	(703/17).CCLS.	USPAT	OR	OFF	2005/04/16 17:49
L7	50	6 and (event and schedul$6)	USPAT	OR	OFF	2005/04/16 17:49
L8	0	7 and non-order	USPAT	OR	OFF	2005/04/16 17:49
L9	44	7 and order	USPAT	OR	OFF	2005/04/16 17:50
L10	50	7 and (order$5 or sequence)	USPAT	OR	OFF	2005/04/16 17:50
L11	0	10 and non-preserving	USPAT	OR	OFF	2005/04/16 17:50
L12	0	10 and (non same preserving)	USPAT	OR	OFF	2005/04/16 17:50
L13	10	10 and (non same order)	USPAT	OR	OFF	2005/04/16 17:51

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Terms used **non order real number event**

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1 Network aware time management and event distribution
George F. Riley, Richard Fujimoto, Mostafa H. Ammar
May 2000 **Proceedings of the fourteenth workshop on Parallel and distributed simulation**

Full text available: pdf(794.39 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we discuss new synchronization algorithms for Parallel and Distributed Discrete Event Simulations (PDES) which exploit the capabilities and behavior of the underlying communications network. Previous work in this areas has assumed the network to be a Black Box which provides a one-to-one, reliable and in-order message passing paradigm. In our work, we utilize the Broadcast capability of the ubiquitous Ethernet for sync ...

2 Fault-tolerant wait-free shared objects
Prasad Jayanti, Tushar Deepak Chandra, Sam Toueg
May 1998 **Journal of the ACM (JACM)**, Volume 45 Issue 3

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Wait-free implementations of shared objects tolerate the failure of processes, but not the failure of base objects from which they are implemented. We consider the problem of implementing shared objects that tolerate the failure of both processes and base objects.We identify two classes of object failures: responsive and nonresponsive. With responsive failures, a faulty object responds to every operation, but its responses may be incorrect. With ...

Keywords: MIMD, asynchronous computing, fault-tolerance, implementation, shared memory, shared objects, synchronization

3 Formal verification in hardware design: a survey
Christoph Kern, Mark R. Greenstreet
April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

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